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Research involving devices incorporating oxides formed by the wet oxidation of Al(Ga)As and $AlAs_{0.56}Sb_{0.44}$ has been performed. Previous results from research on GaAs-On-Insulator (GOI) MESFETs suggested a correlation between channel electronic characteristics, oxidation, and buffer layer. In our research it was found that devices with high aluminum composition LT AlGaAs buffers maintained better channel characteristics after oxidation. In addition to MESFETs, preliminary work into high-speed HBTs was also performed. Base-collector with partially oxidized collectors were found to have a lower capacitance than their unoxidized counterparts. Using a simple capacitive network the reduction in junction capacitance was modeled. Preliminary work was also performed in the InP lattice-matched material system to determine the viability of oxides produced from $AlAs_{0.56}Sb_{0.44}$.

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Introduction

In the silicon material system, the incorporation of an insulating oxide into electronic devices has been shown to produce new devices, such as the MOSFET, and increase device performance/efficiency, Silicon-On-Insulator (SOI) technology. Since the development of the oxide/silicon technology, the "Holy Grail" for III-V semiconductor research has been the addition of an oxide into the III-V material system, which would offer the same benefits as though seen in the silicon material system.

Recently, with the advent of III-V electronics, which incorporate oxidized Al(Ga)As (Al_xO_y), research efforts have been directed toward understanding the oxide, from its formation to its structural and electrical properties. Many have examined the oxidation process that forms Al_xO_y as well as the its structure, but few have studied the electrical properties of the oxide and its effect on the electrical characteristics of electronic devices . For example, the integration of an oxide as an insulating buffer in GaAs field-effect transistors (FETs) has greatly improved the power-added efficiency of that device resulting in record values , but as a result of the oxidation the maximum current level of the device is reduced

In our research we have examined the electrical and structural properties of oxidized $AlAs_{0.56}Sb_{0.44}/In_{0.53}Ga_{0.47}As$ and $Al_xGa_{1-x}As/GaAs$ (x = 0.90 ~ 1.0) interfaces and their impact on electronic devices. Structures similar to FET and heterojunction bipolar transistor (HBT) devices incorporating Al_xO_y have been examined. Aspects of the oxidation process as well as the electrical properties of the devices were analyzed.

$AlAs_{0.56}Sb_{0.44}/In_{0.53}Ga_{0.47}As$

After the success of the application of oxidized Al(Ga)As as an insulating buffer in GaAs MESFETs [ref.] our interest was directed toward reproducing that success in the InP material system with InGaAs HEMTs. Before such devices can be fabricated, the nature and characteristics of the oxide formed from $AlAs_{0.56}Sb_{0.44}$ (AlAsSb), which is latticed matched to InP (Fig. 1), must be examined.

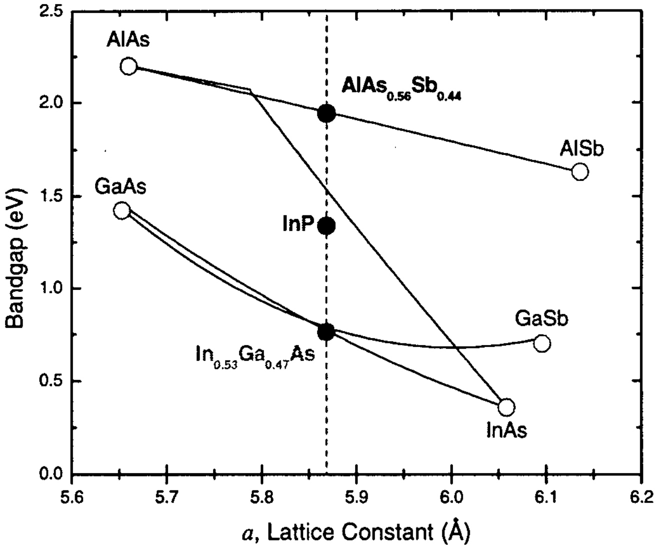
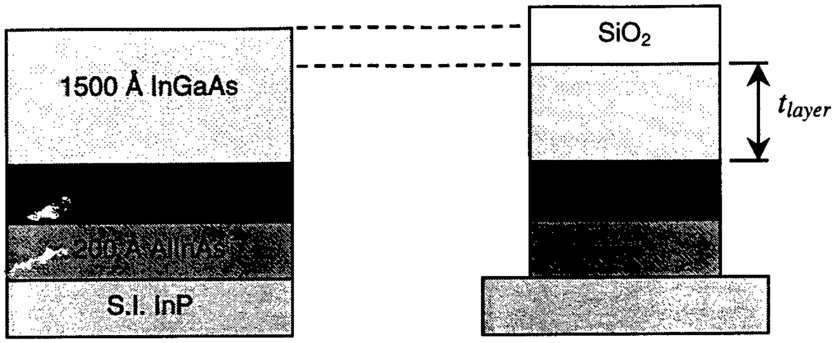


Fig. 1. Bandgap versus Lattice Constant

Oxidation of AlAsSb was carried out in a three-zone open tube quartz furnace, capped at the open end. De-ionized water heated to 90 °C is bubbled into the furnace using nitrogen as the carrier gas. Samples, when ready for oxidation, were placed on a quartz boat, pre-heated to furnace temperature, and positioned in the steam environment of the furnace. In the early stages of work it was found that there was an apparent dependence of the lateral oxidation on the material above the AlAsSb layer being oxidized. An experiment was designed to investigate this phenomenon.

Samples were grown by solid-source molecular beam epitaxy (MBE). The structure (from substrate up) consisted of a semi-insulating InP substrate, 200 Å $Al_{0.48}In_{0.52}As$ buffer grown at 530 °C, 500 Å $AlAs_{0.56}Sb_{0.44}$ layer for oxidation grown at 480 °C, and a 1500 Å $In_{0.53}Ga_{0.47}As$ doped n-type grown at 510 °C. The beam equivalent pressures (BEPs) of As_2 and Sb_4 during the growth of the AlAsSb layer were 1×10^{-6} Torr and 2×10^{-6} Torr. The InGaAs layer was then etched using H_3PO_4:H_2O_2:H_2O (3:1:50 volume ratio) to three additional heights for a total of four: 1500 Å (unetched), 1000 Å, 500 Å, and 250 Å. 2000 Å of silicon dioxide (SiO_2) was then deposited using a plasma enhanced chemical vapor deposition (PECVD) system for use as a reactive ion etching (RIE) mask. The SiO_2 layer was patterned using standard photolithography and SF_6:Ar:O_2 (5:1:2 sccm) RIE. Mesas were then defined in the InGaAs/AlAsSb/AlInAs material structure using chlorine (Cl_2) RIE. Fig. 2 shows the layer structure and completed experimental structure.



a. b.

Fig. 2a. Layer Structure
Fig. 2b. Experimental Structure

Oxidations were carried out at furnace temperatures of 325 °C, 340 °C, 350 °C, 360 °C, 375 °C, 400 °C, 425 °C, and 450 °C. Since there is a distinct color change between the unoxidized and oxidized material due to an associated change in index of refraction, the lateral extent of the oxidation was measurable by optical microscope.

Fig. 3 shows the results of oxidations performed at 350 °C, 375 °C, and 450 °C. No oxidation occurred for any InGaAs layer thickness at 325 °C for up to 30 minutes of oxidation time. No appreciable oxidation occurred for the 1500 Å InGaAs layer thickness for any of the oxidation (furnace) temperatures.

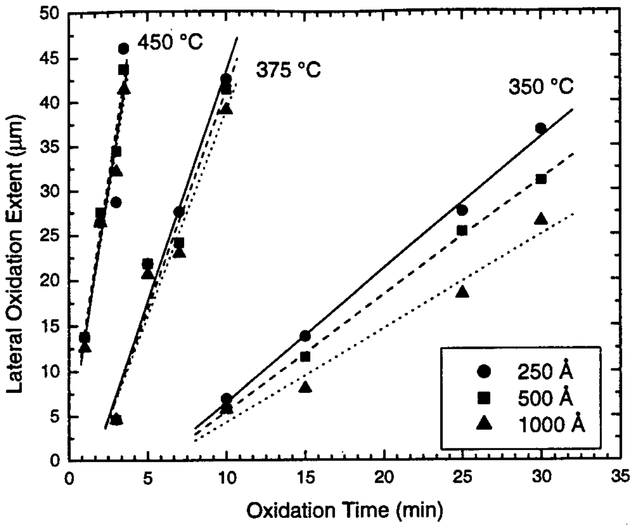


Figure 3 Plot of Lateral Oxidation Extent versus Oxidation Time

Examining Fig. 3 there appeared to be an inverse dependence of the lateral oxidation rate with respect to the overlying InGaAs layer thickness, which becomes less pronounced at elevated temperatures. In Fig. 4 the lateral oxidation rate with respect to overlying InGaAs layer thickness is plotted versus 1/kT. For all thickness the oxidation rate increases with increasing oxidation temperature as expected, until approximately 400 °C at which point the oxidation rate appears to saturate. From Fig. 4 it is clear that at lower oxidation temperatures the lateral oxidation rate is inversely proportional to the overly InGaAs layer thickness, and at higher temperatures that this dependence becomes essentially nonexistent. The two prominent regions in the Arrehnius plot suggest two distinct processes occurring in parallel during the oxidation of the AlAsSb layer: one that is dependent on the overlying layer thickness, dominant at lower oxidation temperatures, and one that is independent of thickness, dominant at higher oxidation temperatures.

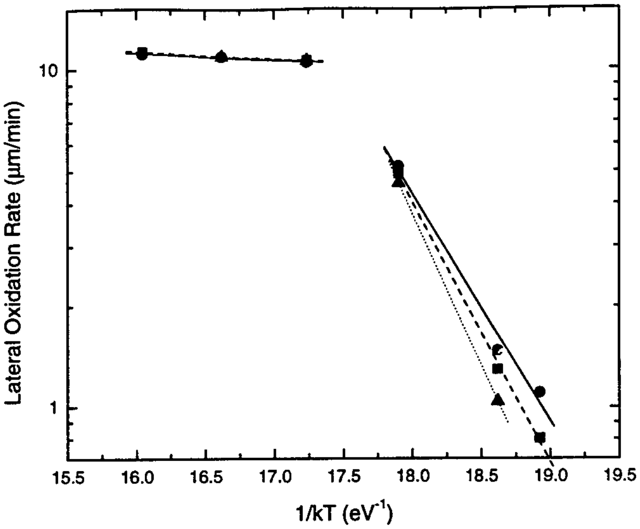


Fig. 4 Arrehnius Plot of Lateral Oxidation Rates

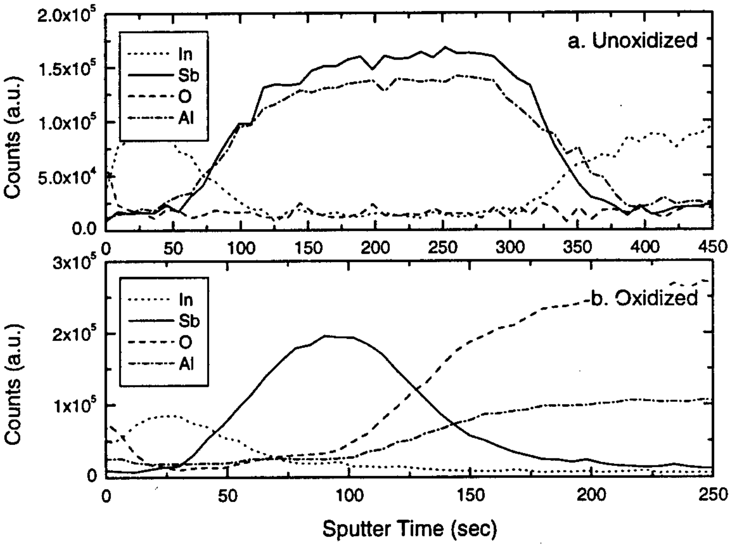


Fig. 5 Auger Depth Profile of a.) an unoxidized sample and b.) an oxidized sample

Using Auger depth profiling it was confirmed that an interfacial antimony (Sb) layer is formed directly above the oxidized material during the oxidation of AlAsSb (Fig. 5a, b). It has also been shown that the total thickness of the oxide/Sb layer is greater than that of the original unoxidized AlAsSb layer [ref.]. This is contrary to the case of an oxide produced from Al(Ga)As, where the resulting oxide layer is thinner than the original Al(Ga)As layer. The thicker oxide/Sb layer deforms the overlying layers with respect to the original unoxidized layer. This strain generates stress in the overlying layers. The energy associated with this stress is proportional to:

$$\varepsilon_{stress} \propto G \cdot t_{layer} \Delta t^2 \tag{1}$$

where G is the shear modulus, t_{layer} is the thickness of the stressed (overlying) layer, and Δt is the deformation. Therefore, we hypothesize that for thicker overlying layers the expected energy required to stress (strain) that layer would increase. Using the Arrehnius model, the approximate activation energies measured for the 250 Å, 500 Å, and 1000 Å overlying InGaAs layers, in the low temperature range, are 2.58 eV, 2.82 eV, and 3.02 eV, respectively (Fig. 4). The trend seen in the activation energies seems to agree with our hypothesis. Additionally, at lower temperatures, where the amount of thermal energy is limited, we would expect that the samples with higher activation energies (thicker overlying layers) would have reduced oxidation rates as compared to samples with lower activation energies (thinner overlying layers). The data presented in Fig. 6 supports this statement.

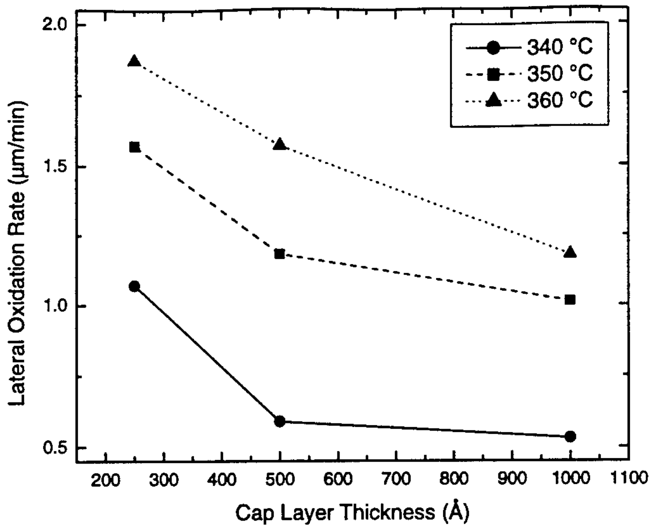


Figure 6 Rate versus Cap thickness

At higher temperatures the amount of the antimony deposited at the upper interface, between the oxide and semiconductor, decreases. This results in a decrease in the amount of strain in the overlying layers, or in other words, decreases the amount of energy required to strain the overlying layers. It is believed that this, in association with the increased amount of thermal energy, reduces the dominance of the overlying layer's thickness over the lateral oxidation rate. Therefore at high enough temperatures the oxidation of the AlAsSb layer can proceed unimpeded and independent of the overlying layer (Fig. 3 and Fig. 4).

Next, to examine the electrical properties of the oxide metal-oxide-semiconductor (MOS) capacitors were fabricated. The MOS capacitor structure was grown by solid-source MBE. The layer structure is presented in Fig. 7.

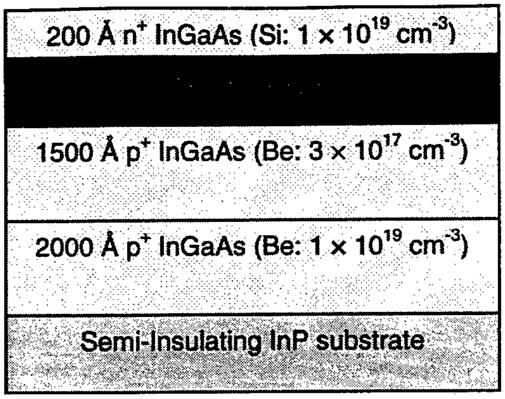

200 Å n$^+$ InGaAs (Si: 1 × 10^{19} cm^{-3})
1500 Å p$^+$ InGaAs (Be: 3 × 10^{17} cm^{-3})
2000 Å p$^+$ InGaAs (Be: 1 × 10^{19} cm^{-3})
Semi-Insulating InP substrate

Fig. 7 Layer structure of InGaAs MOS capacitor

The capacitors were fabricated using two methods. The first consisted of defining a mesa mask in a SiO_2 deposited layer, followed by the definition of the diode mesa using chlorine reactive-ion ecthing (RIE), and the lateral oxidation of the AlAsSb layer, during which the SiO_2 cap layer remained on the sample. The second method consisted of defining a mesa mask in photoresist, followed by definition of the diode mesa using Cl_2 RIE, and the lateral oxidation of the AlAsSb layer, during which there was no cap layer on the sample Following oxidation, Ti/Au contacts are deposited on both samples. See Fig. 8.

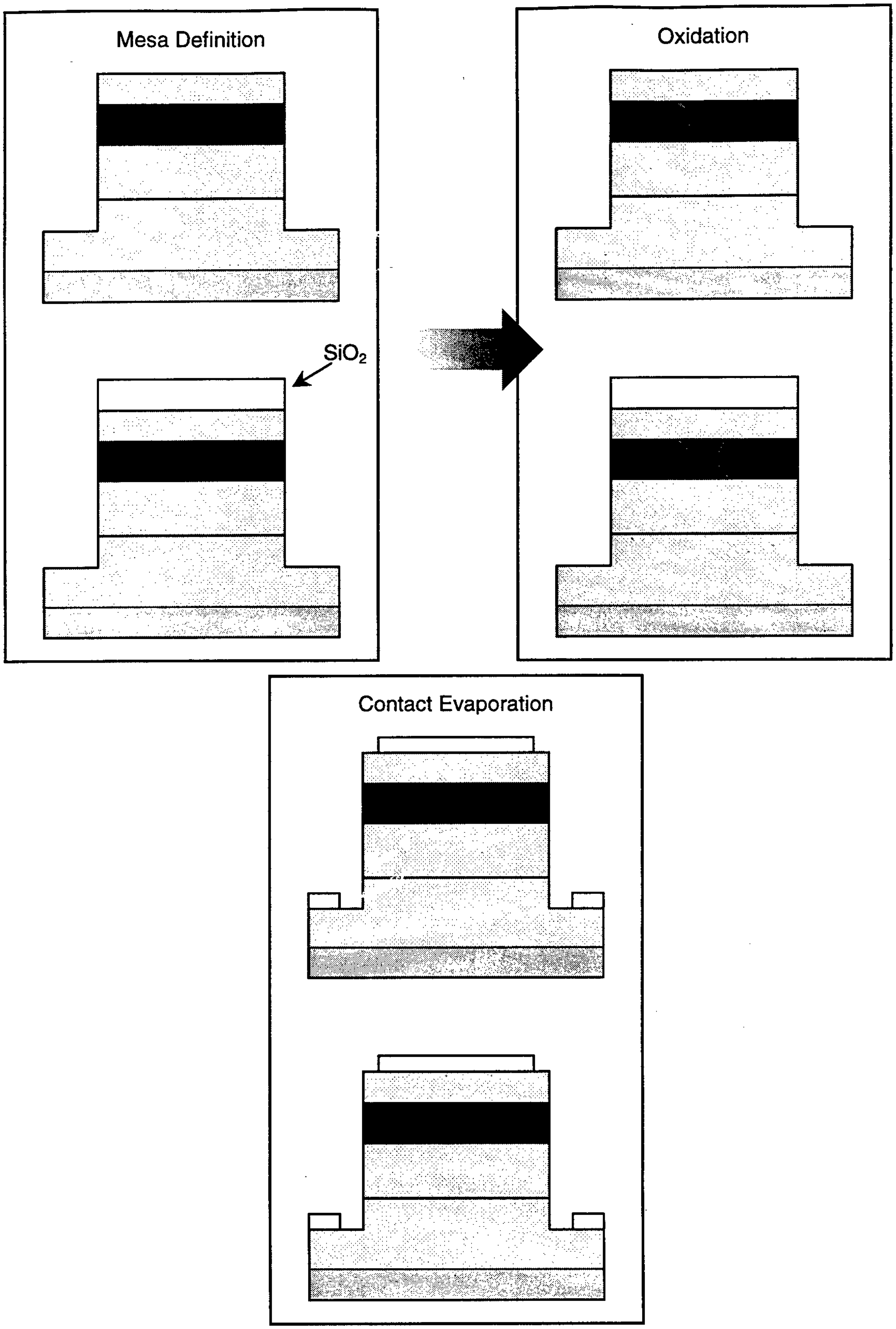
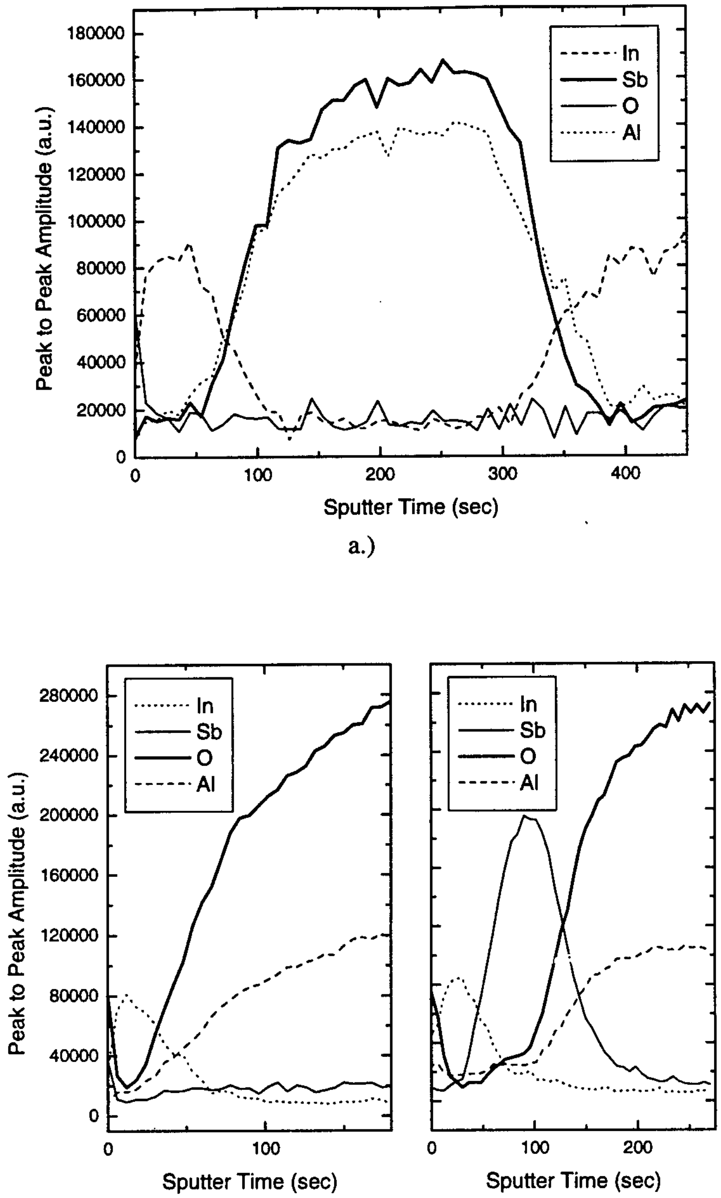

Mesa Definition
Oxidation
SiO2
Contact Evaporation

Fig. 8.

Auger depth profiles of pre-oxidation and post-oxidation samples are presentend in Fig. 9.



a.)

b.)

c.)

Fig. 9 Auger Profiles of Pre-Oxidation and Post-Oxidation Samples

a.) Pre-oxidation

b.) Post-oxidation without SiO_2

c.) Post-oxidation with SiO_2

It is interesting to note that after oxidation the antimony profile differs depending on whether there is a SiO_2 mask present or not. For the sample produced with a SiO_2 mask, there is the distinctive antimony peak at the upper interface, which has been observed by other groups [ref]. For the sample produced without a SiO_2 mask, no antimony peak is present, but there is an low, yet even distribution of antimony throughout the oxide.

The current-voltage characteristics of the two diodes (produced with SiO_2 mask and without) are presented in Fig. 10.

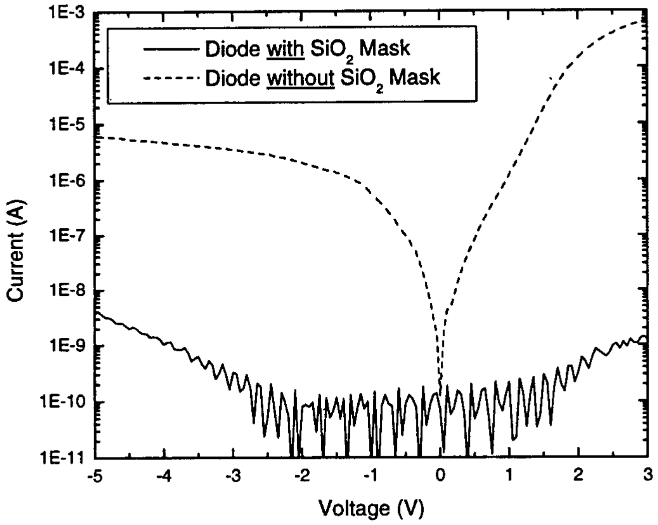


Fig. 10. IV Characteristics of Both Diodes

From Fig. 10 one can see that the sample produced without the SiO_2 mask, which had small amounts of antimony throughout the oxide, has a much higher leakage current, up to six orders of magnitude at some biases. The noise present in the current-voltage characteristic of the sample produced with SiO_2 mask is due to the limit of the measurement device not the device under test. At a 1 V forward bias the current for the sample produced without SiO_2 mask is 12 mA/cm^2 and for the sample produced with

SiO_2 mask is 2.15 μA/cm^2. At a 4 V reverse bias the currents are 47.1 mA/cm^2 and 10.3 μA/cm^2, respectively.

The capacitance-voltage (CV) characteristic of the sample produced with the SiO_2 mask is presented in Fig. 11. CV characterization of the sample produced without the SiO_2 mask was not possible due to its high leakage currents.

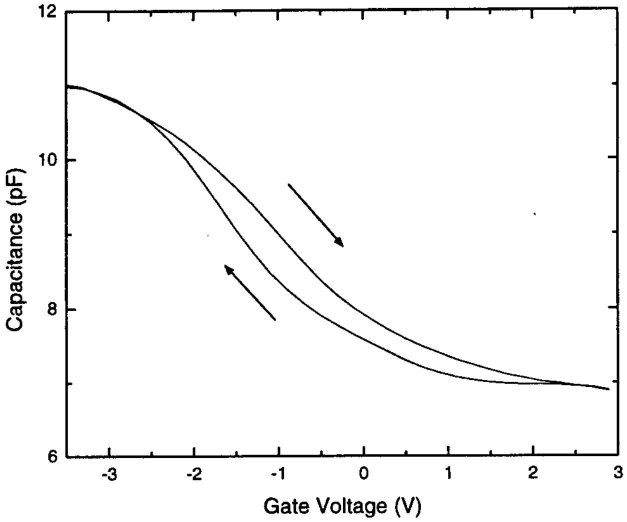


Fig. 11. CV Measurement of
MOS Capacitor

Given that the thickness of the oxide is 500 Å and the area of the diode is 10^{-4} cm^2, the relative permittivity was determined from the CV measurement to be approximately 6.2 ~ 6.3. At this point the origin of the hysteresis is not clear. It could be due to either mobile oxide charge or charge injected into the oxide.

Fig. 12 presents the plot of an ideal CV curve versus the measured CV curve. From the comparison of the ideal and measured curve a flatband voltage shift (ΔV_{FB}) of –1.59 V is measured. From this an oxide charge denisty of 1.1×10^{12} cm^{-2} was calculated.

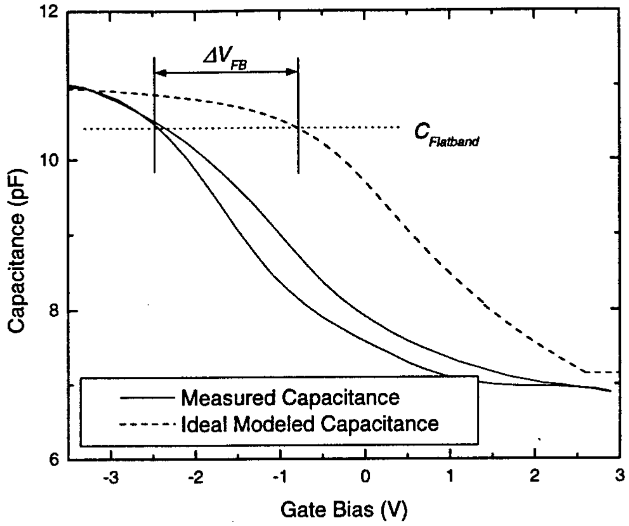


Fig. 12 Ideal CV Curve versus Measured CV Curve

Using the Terman method a dominant trap level spaced approximately 0.1 eV from the valance band was calculated (Fig. 13).

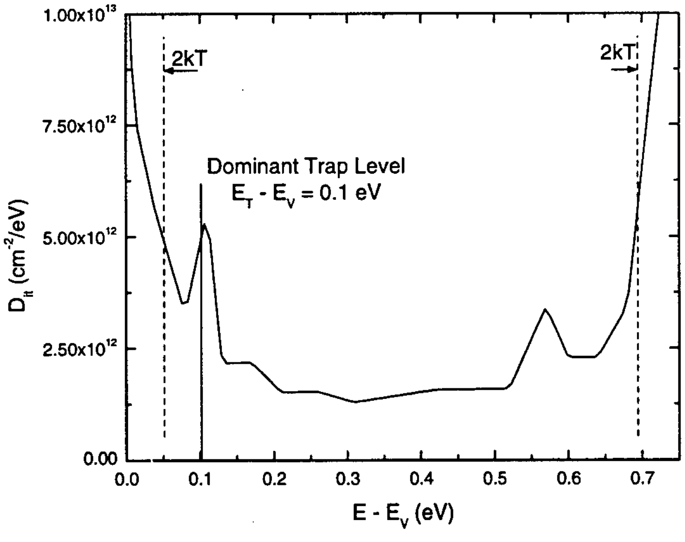


Fig. 13 Graph of results from Terman Analysis

Deep Level Trap Spectroscopy (DLTS), using the Boxcar method, was performed on the MOS capacitor (Fig. 14).

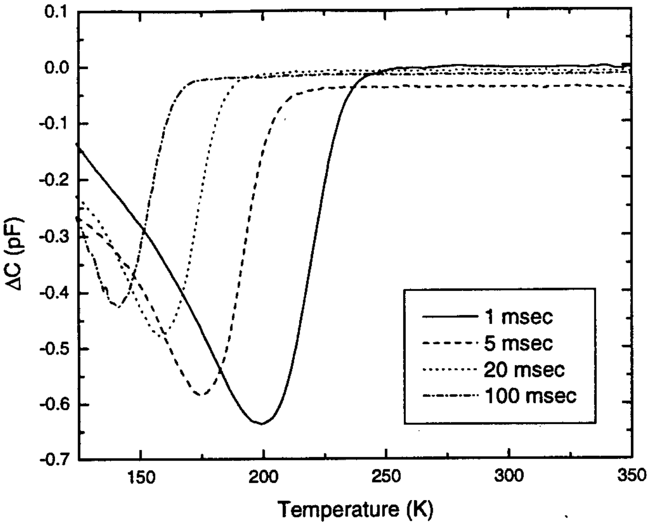


Fig. 14 Boxcar DLTS Scan

The negative ΔC signal indicates a majority carrier trap, in this case a hole trap. From the DLTS scan the energy level of the trap as well as the trap density can be calculated (Fig. 15). From the DLTS scan it was found that the trap energy level ($E_T - E_V$) was found to be 0.15 ~ 0.16 eV, and the trap density (N_T) was found to be 1.2 ~ 1.3 × 10^{12} cm^{-2}.

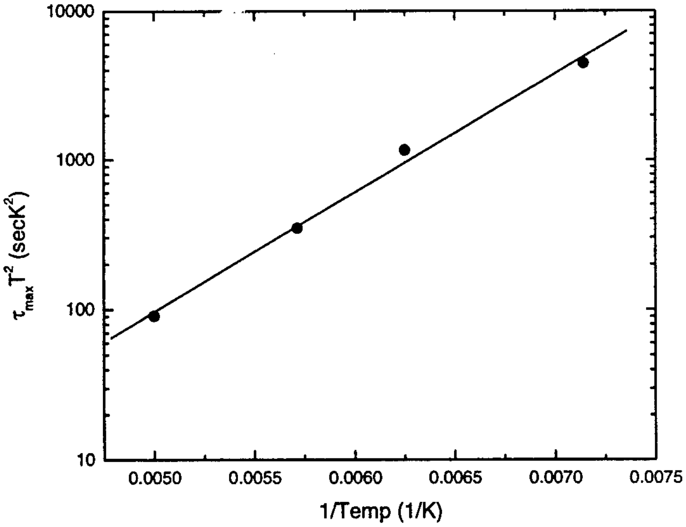


Fig. 15

Al(Ga)As/GaAs

Our most recent work in the area of Al(Ga)As oxides has been concerned with understanding the electrical impact of the oxide. In previous experiements it had been observed that Al(Ga)As layers adjacent to LT Al(Ga)As layers oxidized at higher rates than Al(Ga)As layers adjacent to normally grown GaAs layers. Additionally, it was observed that the GOI MESFETs with oxides formed adjacent to LT Al(Ga)As layers suffered less channel current loss after oxidation. Therefore a series of experiments examing the effect of oxidation on the Hall concetration and mobility of various MESFET structures with LT $Al_xGa_{1-x}As$ (x = 0.0 ~ 0.7) adjacent to the oxidation layer (see Figure. 16) was performed.

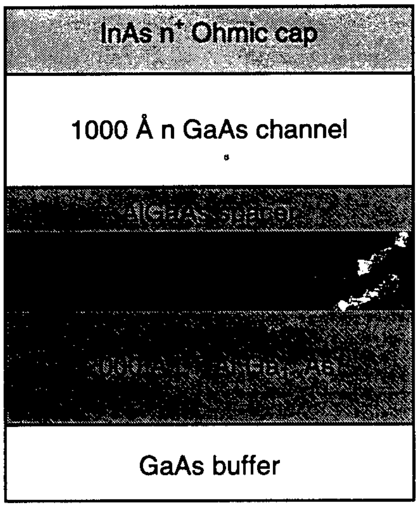


Figure 16. MESFET layer structure

After the samples were grown by MBE, Hall samples, using a Van der Pauw geometry, were fabricated. The samples were oxidized at various temperatures (400 °C, 425 °C, 450 °C). Figure 17 shows the oxidation depth versus time for 425 °C, Figure 18 shows the variation of oxidation rate versus the aluminum composition of the LT AlGaAs layer.

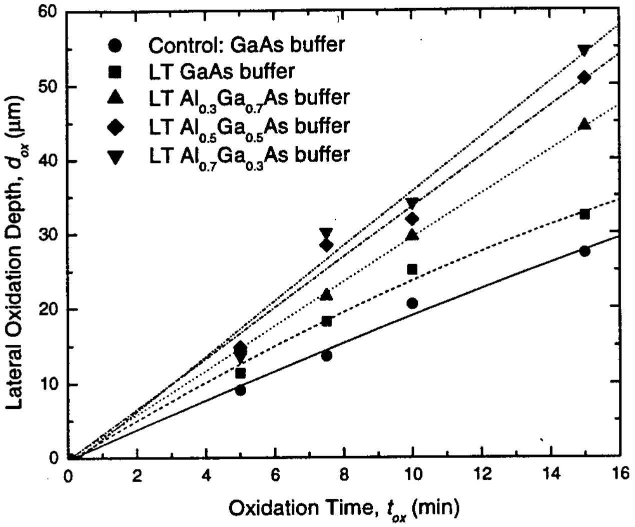


Figure 17. Oxidation depth versus oxidation time

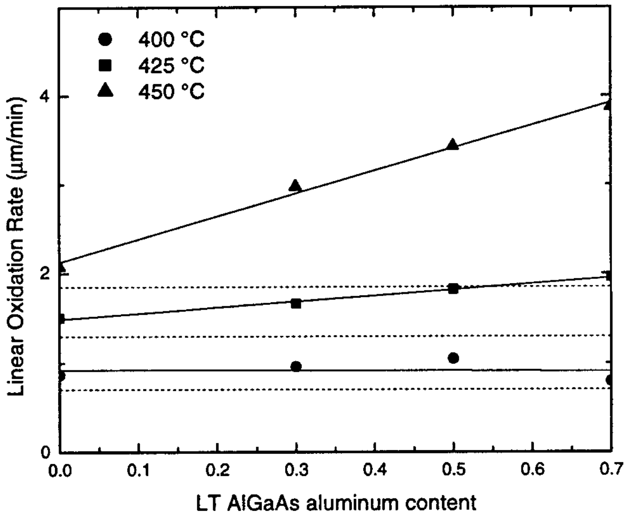


Figure 18. Oxidation rate versus LT AlGaAs aluminum composition

From both Figure 17 and 18 we can see that as the aluminum compostion of the adjacent LT AlGaAs layer is increased, the oxidation rate of the accompanying oxide layer increases.

The following equations are used to normalize the Hall measurement results for comparison:

$$f_n = \frac{n_{ox}}{n_{unox}} \tag{2}$$

$$f_\mu = \frac{\mu_{ox}}{\mu_{unox}} \tag{3}$$

$$f_\sigma = \frac{\sigma_{ox}}{\sigma_{unox}} \tag{4}$$

where f_x is the oxidized x characteristic normalized to its respective unoxidized value, x_{unox} is the value of the characteristic before oxidiation, and x_{ox} is the value after oxidiation. Figures 19, 20, and 21 show f_n, f_μ, and f_σ versus alumiunum composition for the various oxidation temperatures.

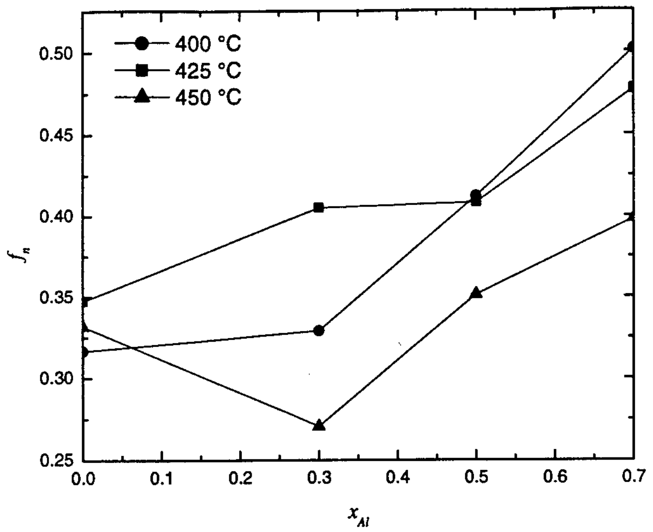


Figure 19. f_n versus aluminum content of LT AlGaAs layer

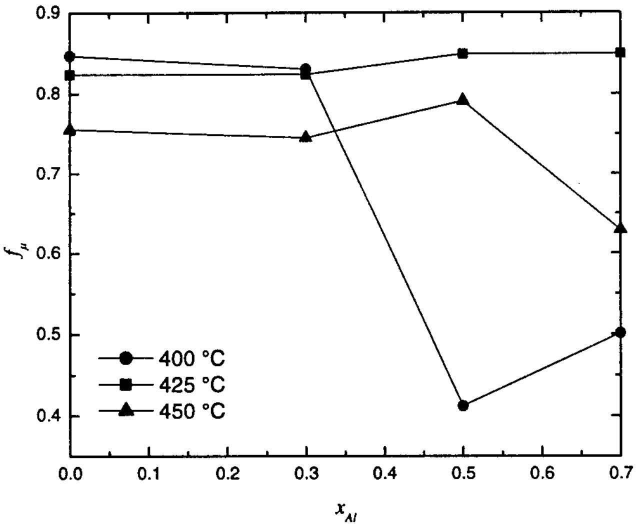


Figure 20. f_μ versus aluminum content of LT AlGaAs layer

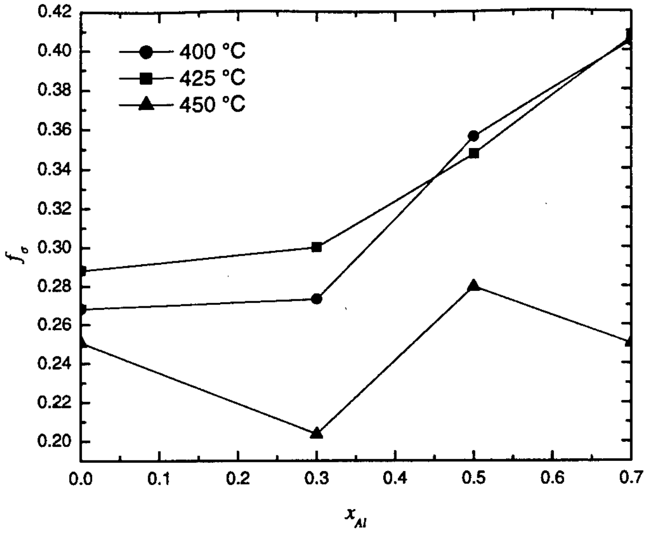


Figure 21. f_σ versus aluminum content of LT AlGaAs layer

From these results, it can be seen as for the higher aluminum composition LT AlGaAs layers, oxidation imposes less of an effect on the channel's electrical characteristics (carrier concentration, mobility, and conductivity).

A summary of this study is as follows:

- Addition of a LT AlGaAs buffer enchances the lateral oxidation of adjacent AlAs layers
- Higher aluminum composition LT AlGaAs buffers result in higher lateral oxidation rates and an increased delay in the onset of the diffusion-limited regime
- GOI MESFET channel current reduction is primarily due to a reduction in the channel's carrier concentration (relative to a small reduction in carrier mobility)
- After oxidation, better channel characteristics were achieved with the higher aluminum composition LT AlGaAs buffer samples thatn compared with the lower aluminum composition samples

In addition to FETs, our work in the Al(Ga)As/GaAs material system has been recently directed towards high-speed heterojunction bipolar transistors (HBTs). Much of the work in developing high-speed HBTs has been directed towards reduceing the base-collector capacitance (C_{BC}) of the device. This is due to the maximum frequency of oscillation's (f_{max}) dependence upon C_{BC}.

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_B C_{BC}}} \tag{5}$$

It is well known that the oxide formed from the steam oxidation of Al(Ga)As has a relative permittivity of approximately 5.8, as compared to GaAs of about 13. Therefore, a HBT with a partially oxidized collector would have a reduce C_{BC} and, consequently, an increased f_{max}. To determine the feasibility of an oxide-collector HBT, several base-collector diodes were fabricated (see Figure 22).

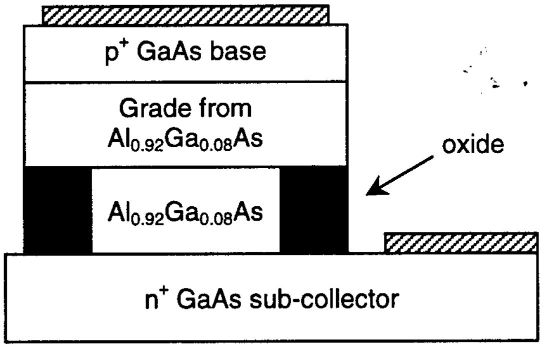


Figure 22. Base-collector diode

The amount of oxide in each diode was varied. It was found that as the amount of oxide in the diode decreased, its capacitance decreased. It is possible to model the capacitance of the structure as a network of parallel plate capacitors (see Figure 23).

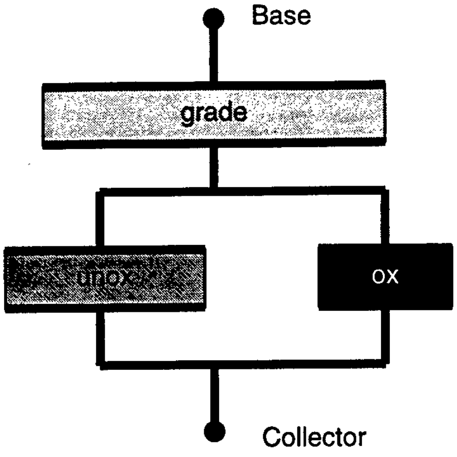


Figure 22. Capcitor network representation of oxide-collector diode.

If we let δ be the ration of the area of the oxide (A_{ox}) to the area of the entire junction (A_C), then the capacitance of the overal structure is given by:

$$\frac{C_{ox}}{C_{unox}} = \frac{\varepsilon_{grade} d_{oxide} + \varepsilon_{oxide} d_{grade}}{\varepsilon_{grade} d_{oxide} + \left[\varepsilon_{unox}(1-\delta)+\varepsilon_{oxide}\delta\right] d_{grade}} \frac{\left[\varepsilon_{unox}(1-\delta)+\varepsilon_{oxide}\delta\right]}{\varepsilon_{unox}} \tag{6}$$

where C_{ox} is the capacitance of the oxidized structure, C_{unox} is the capacitance of the unoxidized structure, d_{oxide} and d_{grade} are the thickness of the oxide and grade layers, relatively, ε_{unox}, ε_{oxide}, and ε_{grade} are the relative permitivities of the unoxidized portion of the diode, the oxidized protion, and the graded layer, and δ is given by:

$$\delta = \frac{A_{ox}}{A_C} \tag{7}$$

Figure 23 shows the measured values versus the model.

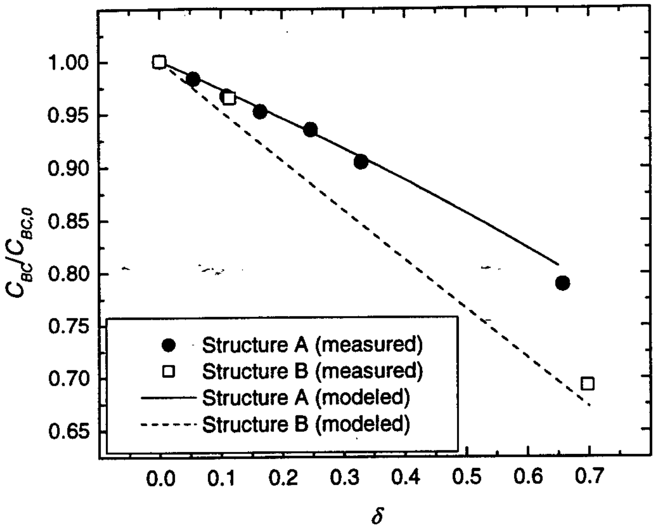


Figure 23. Plot of Cox (normalized to Cunox) versus d

From Figure 23 it can be seen that the capacitance of the junction does decrease and is predictable. At this point, no further research has been performed on HBTs.

Future Work

Future research will be directed to developing high-speed HBTs incorporating oxide apertures in both the Al(Ga)As/GaAs and InP lattice-matched material systems.